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FIND OUT HOW TO GET THE MOST FROM YOUR SOC DESIGN FOR MEETING MULTIPLE POWER NEEDS.

In today's convergence world, the complexity of the system demands a lot from the supply and management of power. The world of a single high-power lossy regulator for supplying power to the whole system is long gone by. A typical portable system has a multiplicity of regulators "both in type and in numbers. As System-on-Chips (SoC) provide more to the system in terms of the level of integration, performance and battery-life to the system, integration of power-management into the SoC becomes a natural "low-hanging fruit" to offer to the system-integrators of today. First, let us take a quick look at what actually necessitates such complex power-regulator requirements. For this, it would be instructive to explore the insides of a cell-phone or any other portable gadget. The following figure shows the functions that a high-end portable gadget would integrate.

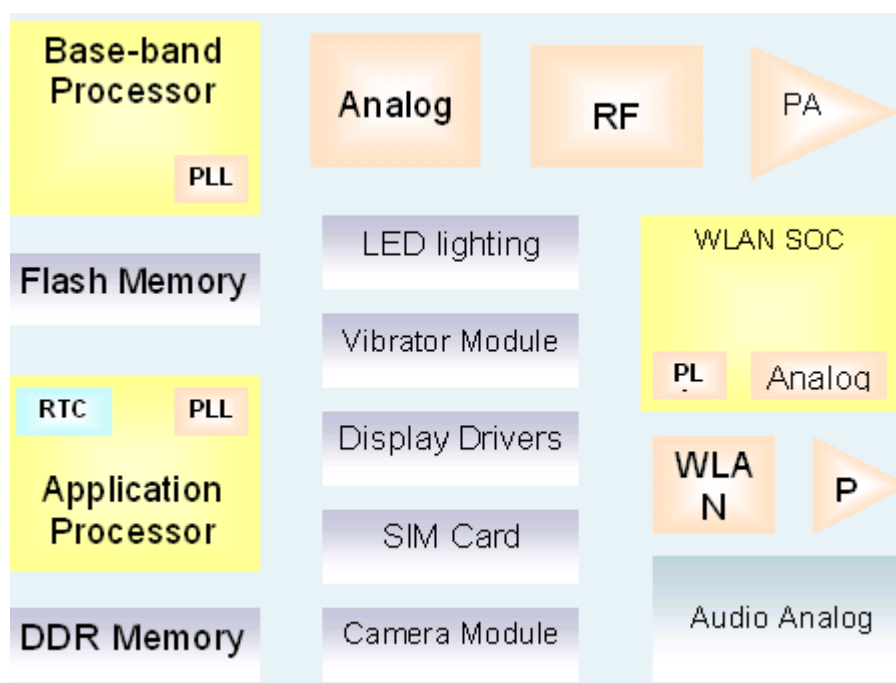


Figure 1: Integrated functions integrated on high-end portable device

We will now see how the power-design for such a complex system can be a significant challenge for the system integrator.

The system integrator's challenges

Requirements challenge:

Such a complex system requires the system integrator to carefully architect and tailor the power requirements to the individual chips and sub-units. The various aspects that a system integrator needs to consider and balance out are truly many.

For instance, the power-sequencing across chips is an issue that requires investigating often undocumented behavior of the chips and modules being integrated. As if this were not enough, the system integrator needs to understand the power-supply requirements for each chip that's being integrated.

Take for instance an "add-on" communication function on a mobile handheld such as a Bluetooth, UWB, WiMax or a WiFi chip " the system integrator needs to identify the power requirements and their interactions for a list of sub-functions that might go like this:

Sub-unit	Example requirements on power
SoC power island-1	1.2V programmable down to 1.0V at 100mA
SoC power island-2	1.0V at 50mA fixed
PLL-power	A fixed 1.2V at 10mA, low-noise
SoC IO power	Fixed 3.3V supply
Analog Front End power	1.2V fixed low-noise power
RF	2.5V fixed voltage at very low noise
PA	Direct connect to the battery

Table 1: Communications power requirements for hand-held devices

An application processor (likely implemented in a different process node requiring different set of voltage levels than the above) would have its own set of power requirements such as the following example:

Sub-unit	Example requirements on power
SoC power island-1	1.1V programmable down to 0.9V at 50mA
SoC power island-2	1.1V programmable down to 0.9V at 50mA
SoC power island-3	1.1V programmable down to 0.9V at 50mA
PLL-power	A fixed 1.1V at 10mA, low-noise
SoC IO power	Fixed 2.5V supply
Real-Time-Clock	A fixed 1.1V at 3mA, always ON
Mobile DDR interface	1.8V power supply

Table 2: Applications processor power requirements

The user-interface functions such as the below listed ones need another set of power supplies:-

Sub-unit	Example requirements on power
Backlighting LEDs	An LED driver power from using a capacitive charge pump, for instance
Power to the SIM-Card	1.8V or 3.3V
Vibrator power	A voltage waveform patterns that drives the motor
Camera Module	A fixed 3.3V supply
Power for the Audio unit	A fixed 3.0V supply that is low-noise and clean

Table 3: User interface power requirements

While the above examples are by no means complete, it was used to illustrate the complexity of the requirements on power that a system-integrator needs to care-about and design for. The voltage, current and noise requirements need to be understood, the depends of one supply on the other, the sharing and the sequencing, the choice of power-regulators, the PCB design, all of which need to be worked out by the system designer. We now take a peek into some of these challenges.

The architecture challenge

The architecting of the power-delivery system needs to deal with a number of challenges. The following are some examples that the system integrator needs to contend with:

1. Sharing of supplies: sharing the 2.5V IO supplies across two chips might look like an innocuous and smart thing to do. Not anymore if the IO power to one chip would need to be shut-down to save power.
2. Noisy versus clean supplies: For a "noisy" digital function, a switching regulator is usually the optimal choice. For a "clean" Analog supply, a linear regulator is a better choice.
3. Making the clean-supply squeaky clean: While a linear regulator does generate a clean supply, elements of a voltage ripple at its input supply can "leak" to the output of the regulator, that might still be sufficient noise to affect an RF LNA performance or to affect the quality of an audio output. In these situations, the linear regulator needs to have a high PSRR to reject the noise.
4. Voltage-islanding: For isolating different digital blocks in an SoC that might need different supply voltage for the purpose of a Dynamic Voltage Management, one is left with making a choice between multiple switching regulators that are more efficient but are more expensive and needing an inductor, versus using a single switching regulator and multiple linear LDO regulators (that are cheaper) following it to fanout into multiple voltage islands.
5. Always-on functions: A function such as a real-time-clock would need to be powered directly from a battery since it needs to be ON all the time. Functions that constantly "listen" to incoming signals or packets would also need to be powered most of the time. Power supply regulators that supply such units may need to derive power directly from a battery.
6. Optimizing the efficiency: While a processing unit in its full-function mode may take, say a 150mA of current, in its most-common mode, the power drawn may be 20mA. In such circumstances, the chosen power-regulator needs to offer a high efficiency at low-current situations.
7. Drop-out: While a linear regulator typically provides a cleaner power than a switching regulator, it suffers from the draw-back of higher power dissipation due to the "drop-out" on its output power transistor. Other than the additional power dissipation, it may mean generation of an additional voltage-line. For example, an LDO that generates a 1.2V supply would need a 1.35V input supply.
8. Power-sequencing: While powering-on, the system integrator needs to ensure the right supplies come ON first so that latch-up or undesirable conditions do not occur. Similar issues exist when switching power-islands ON or OFF. These situations must also occur during the power-down.

The above list of challenges in a system power-design is not exhaustive, but nevertheless indicative of the power-design complexity.

Implementation and production challenges:

Other than the above electrical challenges, there are several important aspects to address:

- Board-level Floor-plan: Proximity of the power-source to the usage point is desirable. This dictates the partitioning and choice of the power-regulator chips.
- Board Layout: Power typically requires islands, taking up valuable board space. This needs to be minimized and managed.
- Choice of inductors and capacitors: Profile, ESR and cost would be typical considerations.
- Choice of vendors: A high-volume system company needs to ensure multiple sources for the power-components in order to ensure a steady supply, and avoiding dependence on a single supplier. This implies qualifying multiple chips.
- Production Sourcing and Vendor management: During production, having to source components from multiple vendors makes the process of sourcing and vendor management very complex.

From the above overview, it would be apparent that the power-system integration into a system is a complex one indeed, and opens up an opportunity for the System-on-Chip

designers to mitigate some of this complexity to the system integrate, and hence offer a true higher value to customers.

The SoC value proposition

Integration of power-management functions on to the SOC comes to the rescue of the system-integrators challenge. We now consider the optimization goals for a typical System-on-Chip design, and then go on to discuss how power-management integration addresses each of these SOC value propositions.

- to achieve lowest cost
- a high level of integration and hence save PCB space
- require cost-effective components
- modularity
- ease of integration (plug-n-play), and,
- ease of production sourcing to the system company
- minimal support
- reduced integration cycle-time

Satisfying all of these goals would be a means to getting the SoC designed into a customer reference platform. It will be shortly apparent as to how integrating power regulators into System-On-Chips positively impacts all of the above goals.

Power-ON SoC

We consider an example system-on-chip that implements an add-on communication function such as supporting WiFi, UWB or WiMax, and outline a scenario of power-integration that would make it a system-friendly chip.

Such a typical system-on-chip has the following functional blocks that need specific power-design:

- The main digital core logic island: Consisting of digital gates running either in active mode or sleep mode, or at modes of intermediate clock-frequencies, a programmable power-supply is needed. The power regulator needs to be efficient since this block typically adds significant power consumption to the system power-budget.
- A real-time-clock logic or wake-up logic island: This block is always ON, either keeping real-time, or ready to respond to requests by the user or the host processor or from the external environment (such as a received packet). The power consumption is typically low, but being active always, the power-supply for such a block also needs to be of intrinsically low power consumption. A fixed power-supply voltage is usually sufficient.
- Digital IO: The power for the IO ring of the chip, needing either, 1.8V, 2.5V or 3.3V or potentially a combination of these voltages. The noise on the supply is unimportant, while the efficiency is still important.
- PLL Power: There could be one or more PLL blocks used in an SoC that might need a low level of power, but a relatively clean supply to keep the jitter of the clock at a minimum.
- Analog Front End: This needs a low-noise power supply, and typically consumes a constant amount of current. The efficiency would typically need to be optimized for a small range of load currents. An LDO regulator with sufficient power-supply rejection becomes necessary.
- RF section: Typically needs a very low noise supply, and a low-noise linear regulator becomes a must.
- Power-amplifier: Could be powered off the battery or off a switching supply with programmable voltages, with the programmability typically used to save power for lower power transmissions.
- Auxiliary power: Typically required for powering support functions such as LEDs or power to bus-powered peripherals such as USB.

The following diagram illustrates a typical integration of a set of power-regulators needed for such an SoC.

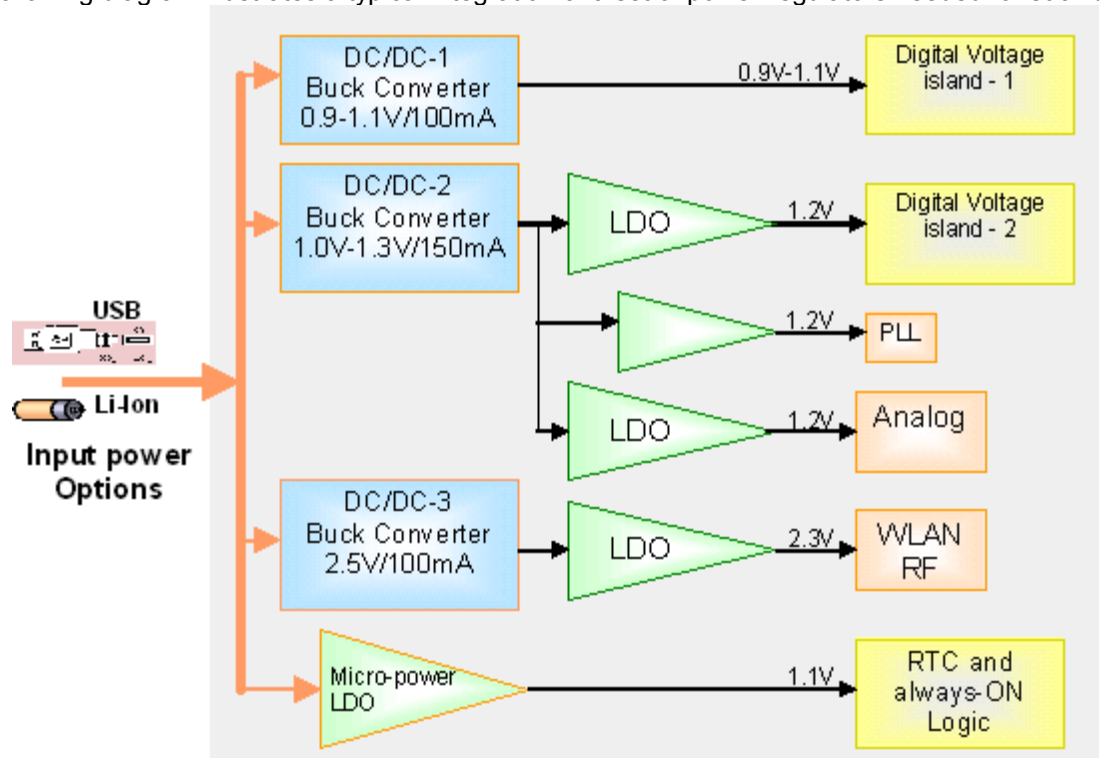


Figure 2: Typical integration of power regulators for SoC

Value

We shall now examine the value of such integration on the SoC.

Cost

Contrary to common-belief, the die-size of the power-regulators especially for portable applications is fairly small. For example, in the 90nm process, a buck-regulator that supplies 1.2V and 200mA would be less than 0.5mm². Including test-cost, an estimate for the additional cost would be around 5cents, compared to over 110-20cents for the discrete part.

The difference becomes more dramatic when a PMU sub-system with multiple DCDC converters is integrated. For example the cost differential between an integrated PMU of size 3mm² versus an external PMU solution could be more than a dollar.

Space

PMU integration on to the SoC could eliminate several power-management chips on the board. The total area savings could range from 5mm² all the way to a cm² of board space savings.

Optimality and Performance

With an integrated tailor made PMU solution, the constraints imposed by available power-management chips are eliminated. One could architect most optimal power-management scenario exactly suited to the SoC system.

For example, the load current at which the efficiency needs to be maximized for, or the frequency at which

the PSRR of an LDO regulator needs to be optimized for, or the voltage values themselves could be tailored exactly per the system requirements. Another example for would the sequencing of the power that can be tailored to the system.

Software

Once the power-management is integrated on to the SoC, the software knows exactly about the power-system. It is no longer a variable dependant on the system-integrator. This allows software stack to be developed exactly tailored to the chip, thus making it easy for the system-software integrator.

Plug-n-play power

With the complete power-hardware and software needed for an SoC integrated on-chip, all it would take is a single primary input supply to be connected to say, a battery or USB power or the power adapter. Hence the power-system integration becomes plug-n-play for the system integrator. The modularity and completeness of the SoC allows easy design-in as an add-on to the system, with minimal changes for the system integrator.

Procurement

Not the least, the elimination of several small power-management chips on the board helps minimize the number, the kind and the companies from which the system integrator would have to procure the components. The design-in of the SoC with power-integration minimizes the additional collateral burden on procurement.

Conclusion

Today's power-system design is complex, with multiple supply voltages, currents and noise requirements for the multiple System-on-chips sued in the system. The system-designer has to contend with multiple challenges that becomes a challenge and opportunity for a system-on-chip to eliminate. Power-regulator integration is a natural progression in the level of integration. A compelling value-proposition exists for power-regulator integration that includes significant cost, board-space, software, performance and modularity advantages.

As more and more System-on-chips integrate power-regulators, it is expected to become a main-stream in most chips, especially in the portable consumer space. The existence of a wide portfolio of silicon proven power-regulator IP cores has become a necessity in the industry today, and Cosmic Circuits Power-ON-SoC silicon-proven family fills this requirement.